High Speed Lateral Power Devices

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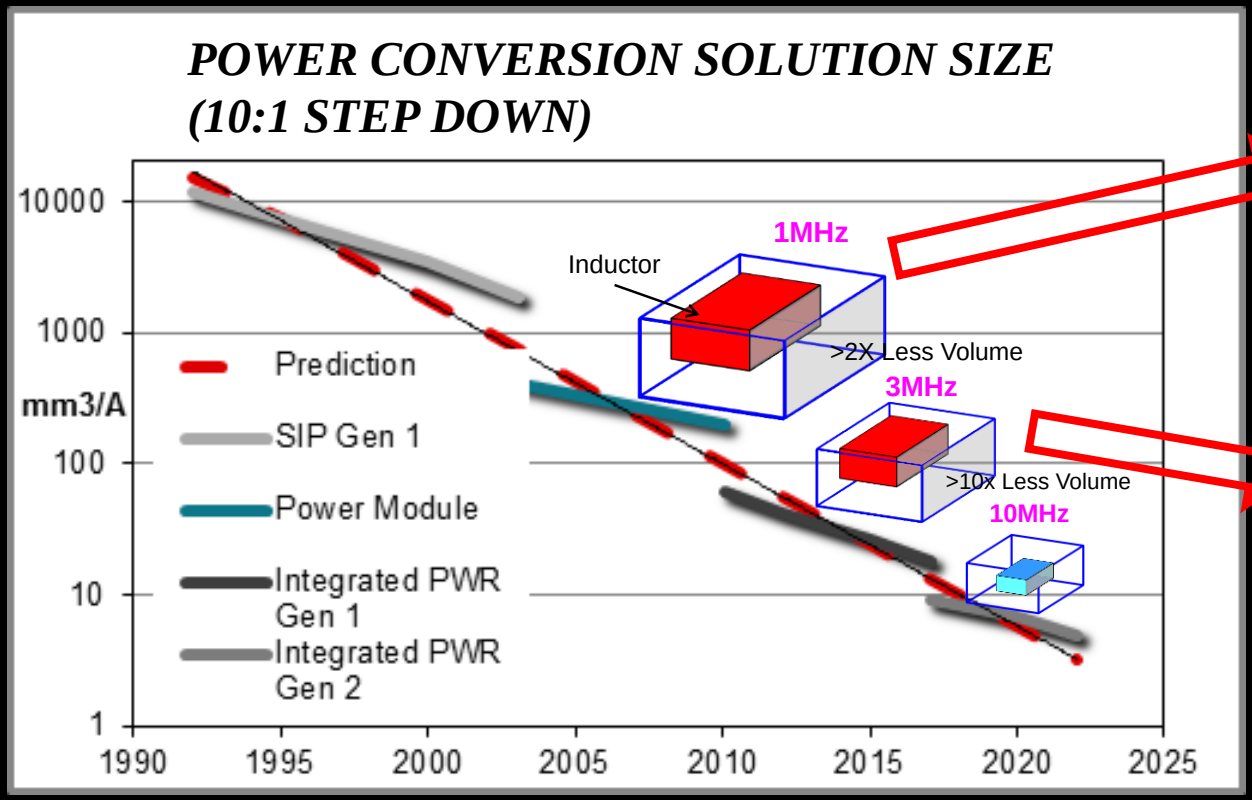
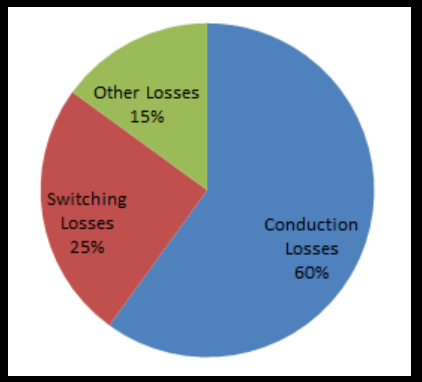
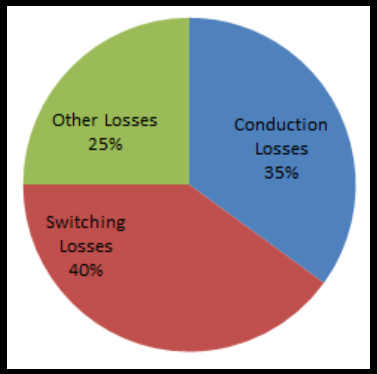
Outline

- Integrated LDMOS
- Isolation Requirements
- Interconnect & Packaging
- Discrete lateral DMOS & Packaging
- Summary

High Frequency Switching







- End solution size is the primary driver

Key Power Device Drivers

- Rsp important ➔ Key Si cost driver

BUT

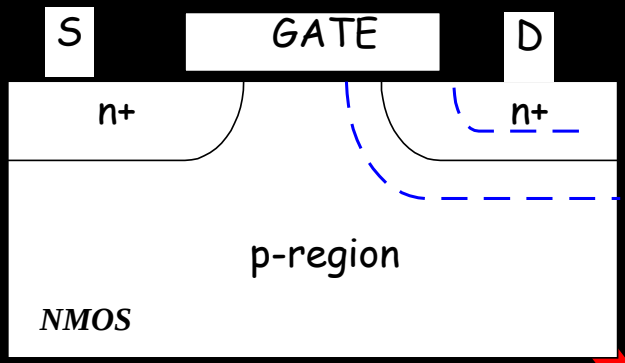
- R x Qtot(Qgd) & Qrr ➔ Key performance drivers and system cost drivers

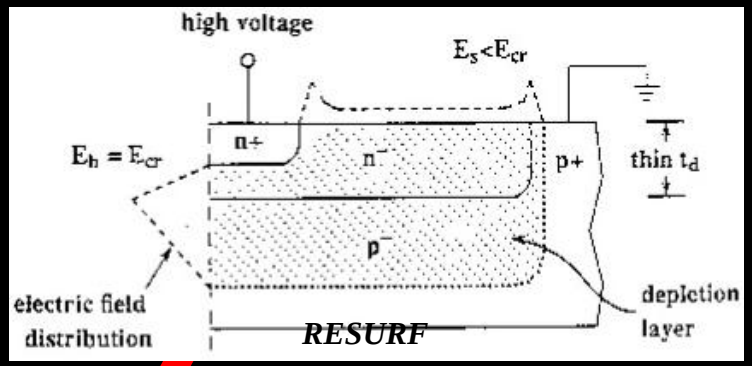
ALSO NEED

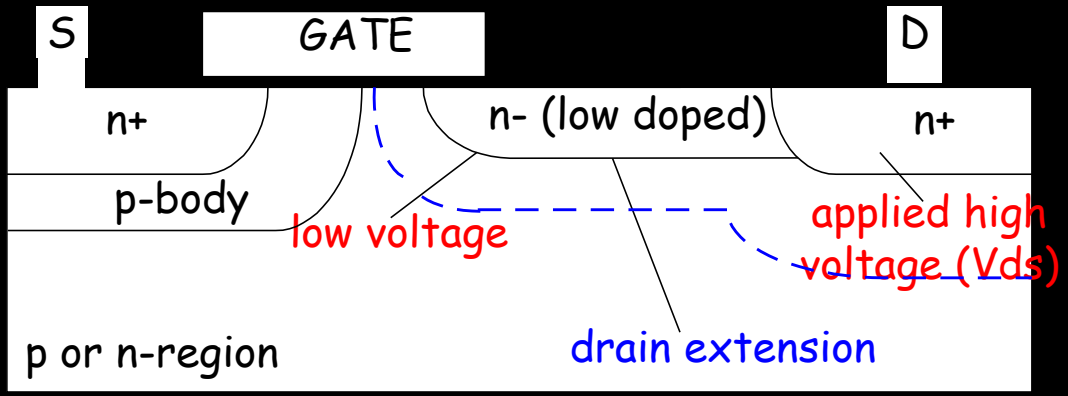
- Reduced parasitics (gate loop and power loop L, CSI)

Integration and Integrated LDMOS

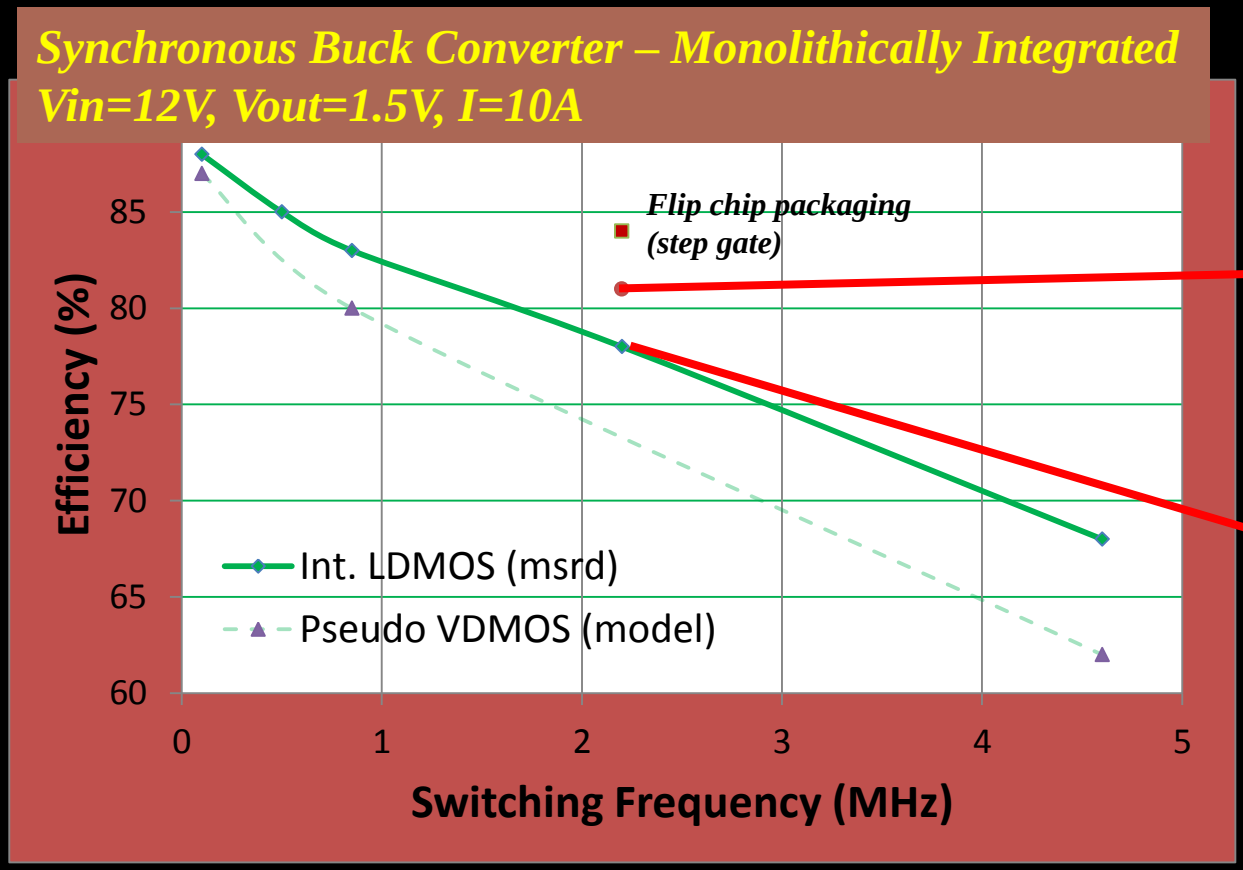
LDMOS

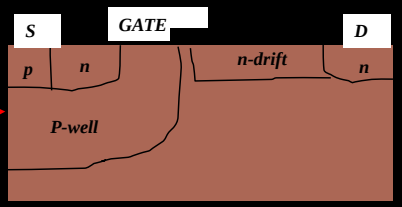

S
GATE
D
n+
n+
p-region
NMOS

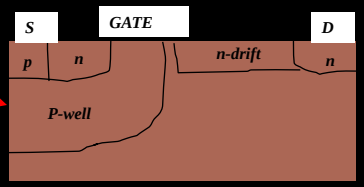

high voltage
$E_s<E_{cr}$
$E_h = E_{cr}$
n+
n⁻
p+
thin t_d
p⁻
electric field distribution
depletion layer
RESURF


S
GATE
D
n+
n- (low doped)
n+
p-body
low voltage
applied high voltage (Vds)
p or n-region
drain extension

LDMOS Benefit

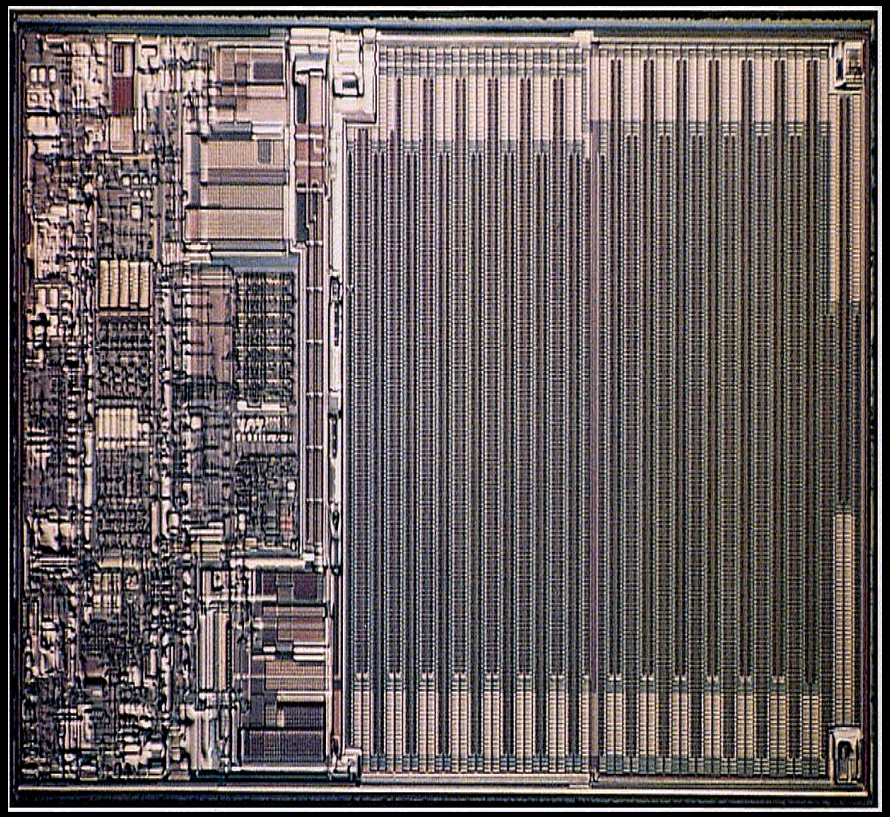


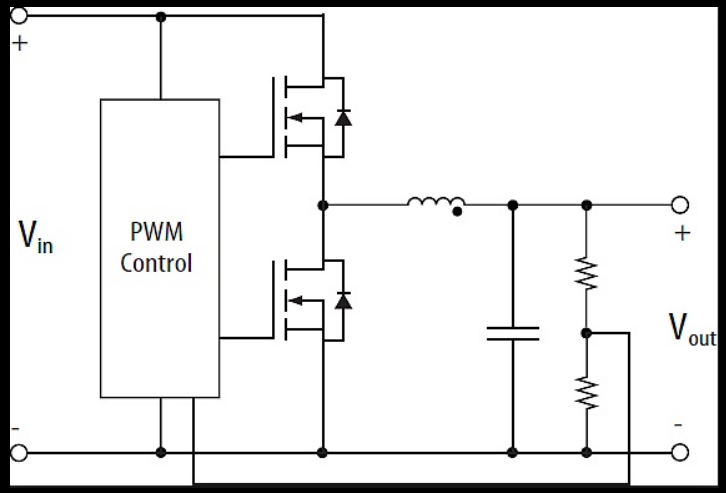




- Multi-voltage, Easy to Integrate
- Lowest Qg/Qtot for given Rdson – monolithically integrated
  - *Low voltage integrated VDMOS not efficient due to significantly high Rsp*

Integrated Power Conversion

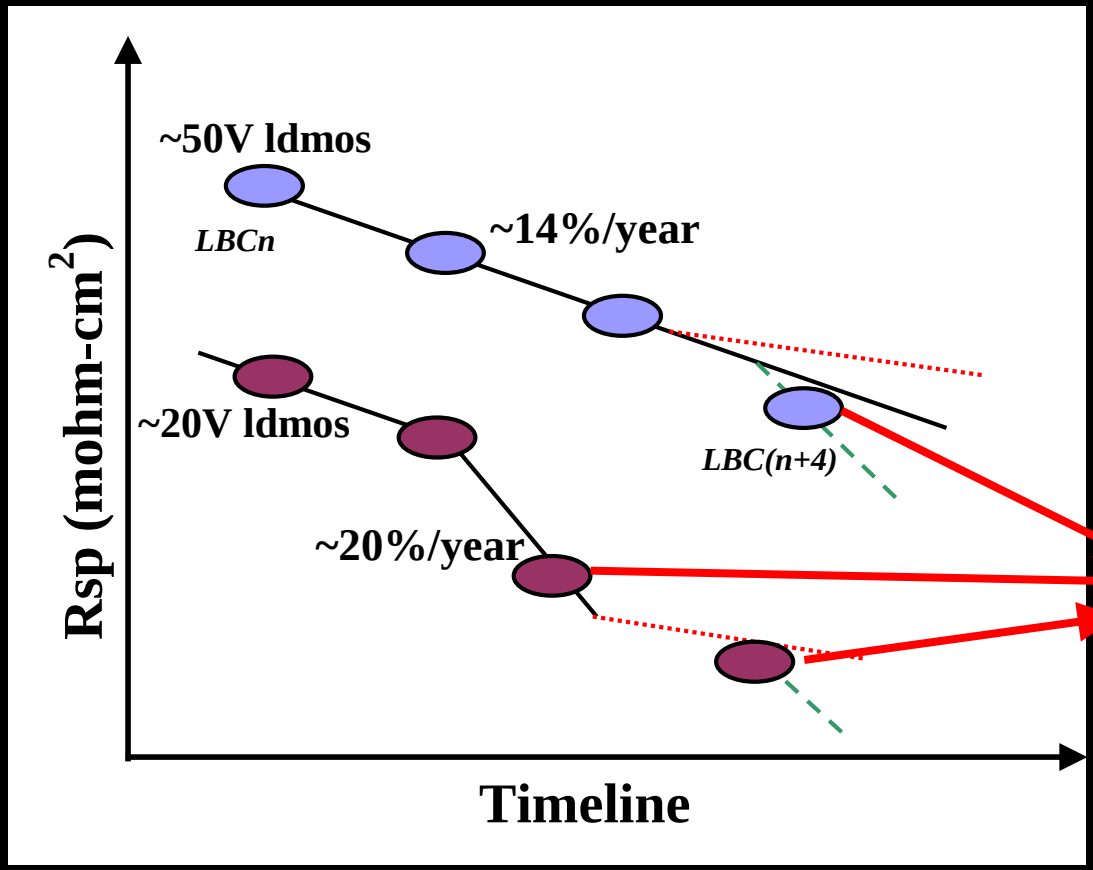




High speed Synchronous Buck Converter

- Monolithic integration helps reduce both gate loop and power loop inductance

Integrated FET Scaling – Drives Technology



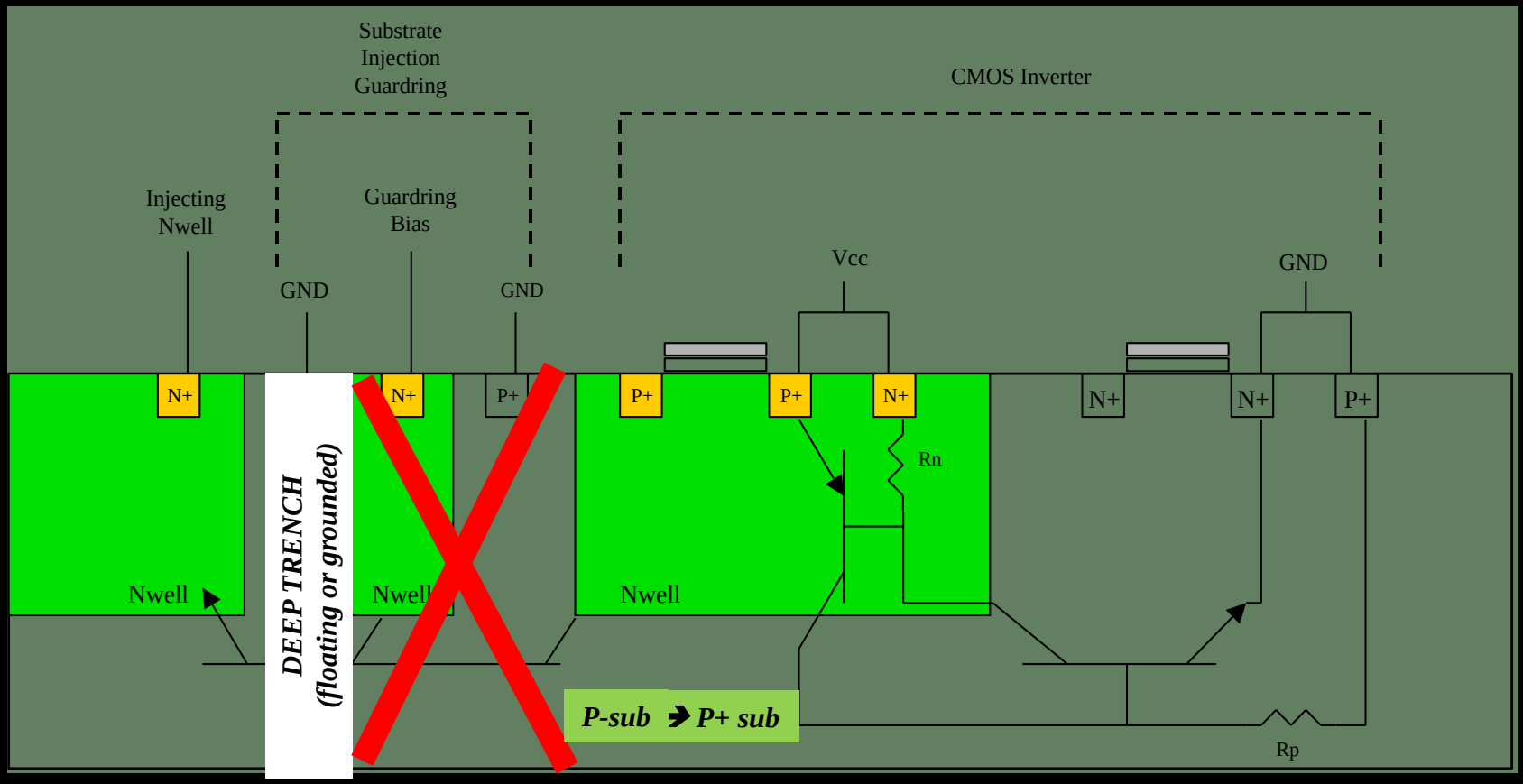
- Integrated FET improvement at TI
  - about 25-30% node-on-node improvement

Outline

- Integrated LDMOS
- Isolation Requirements
  - Functionality
  - Efficiency

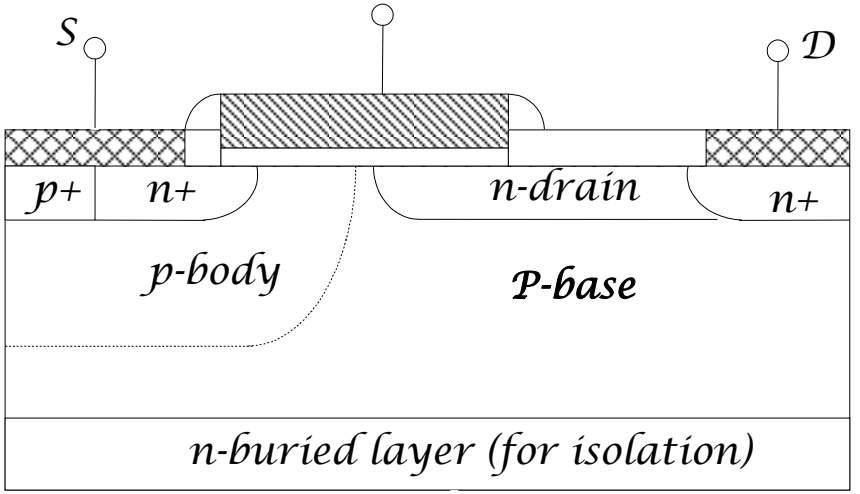
- Interconnect & Packaging
- Discrete lateral DMOS & Packaging
- Summary

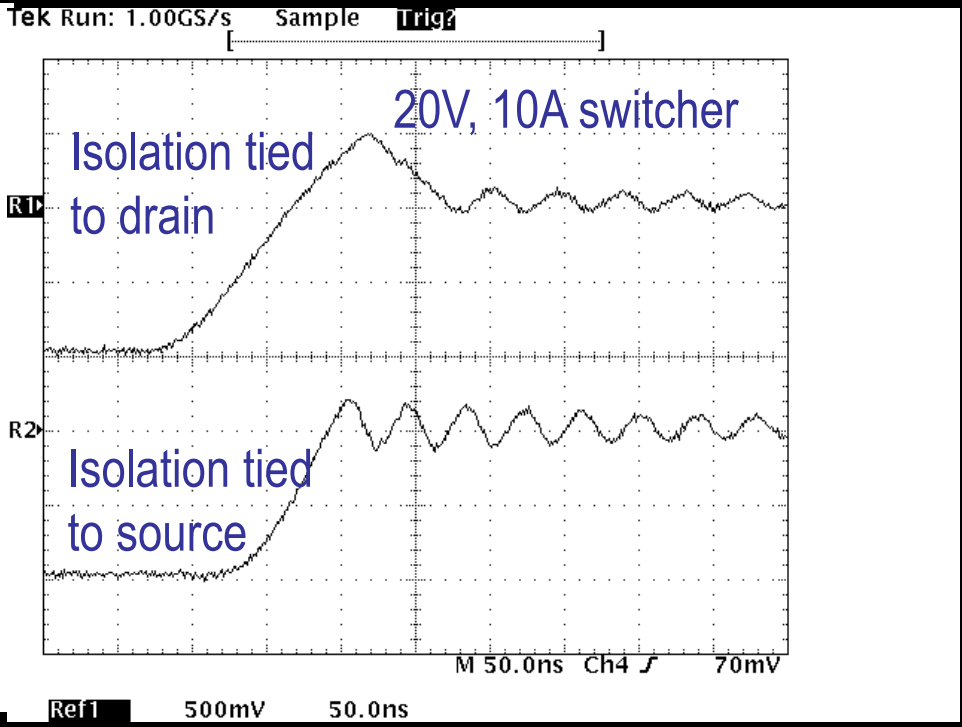
Isolation - Functionality



- Protect circuitry from carrier injection
  - Diode recovery, Substrate bounce/noise

Isolation – Efficiency Improvement



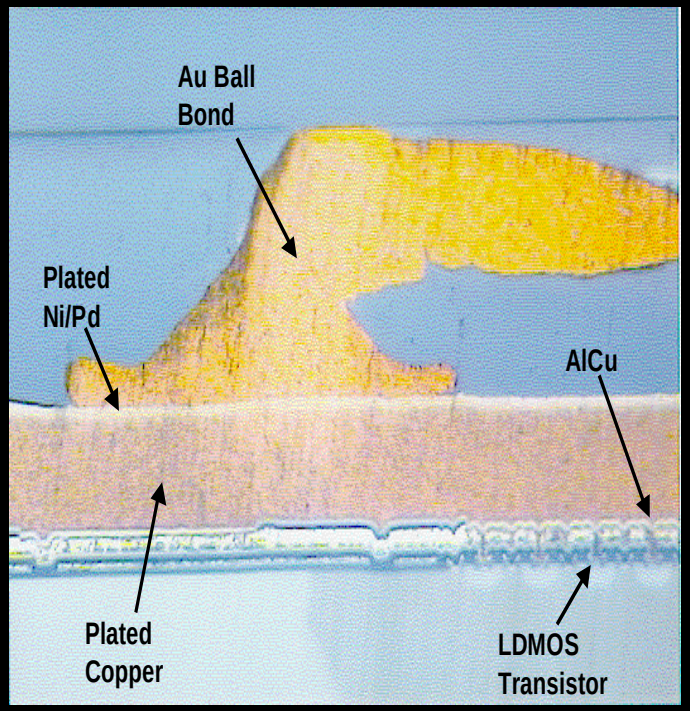


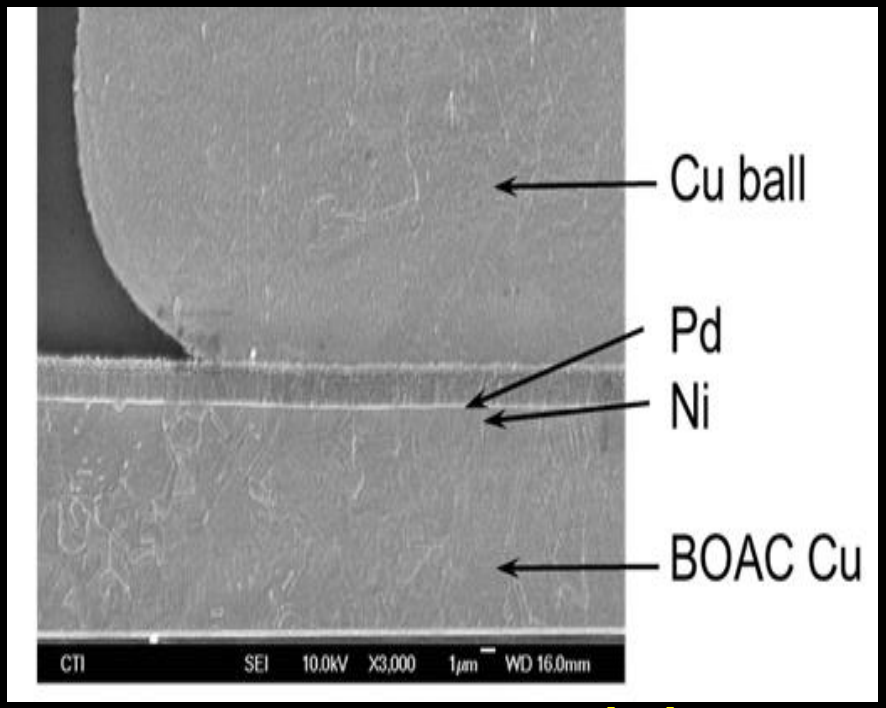
- Integrated guard ring significantly reduces diode recovery loss → **enables faster switching**

Outline

- Integrated LDMOS
- Isolation Requirements
- Interconnect & Packaging
  - Electro migration
  - Parasitic inductance
  - Size and footprint
- Discrete lateral DMOS & Packaging
- Summary

Interconnect Optimization

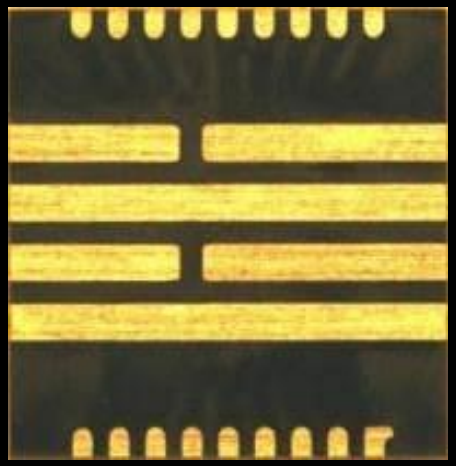




Thick copper and bonding technology

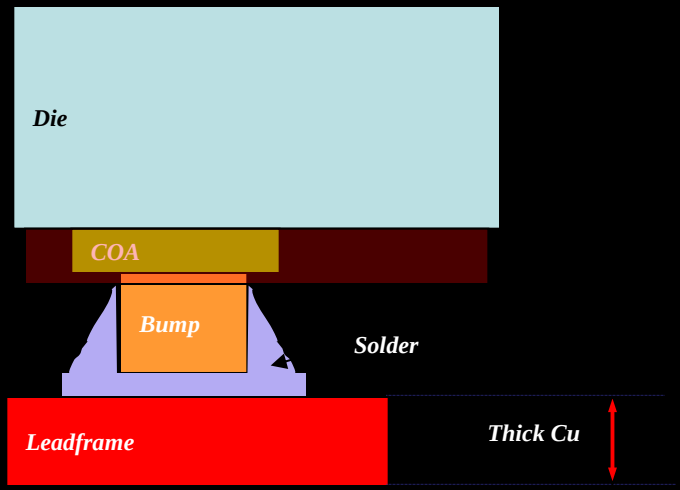
- Thick Copper allows direct bonding on top of active device – delivers distributed current
- Enables flip chip package eliminating bondwires

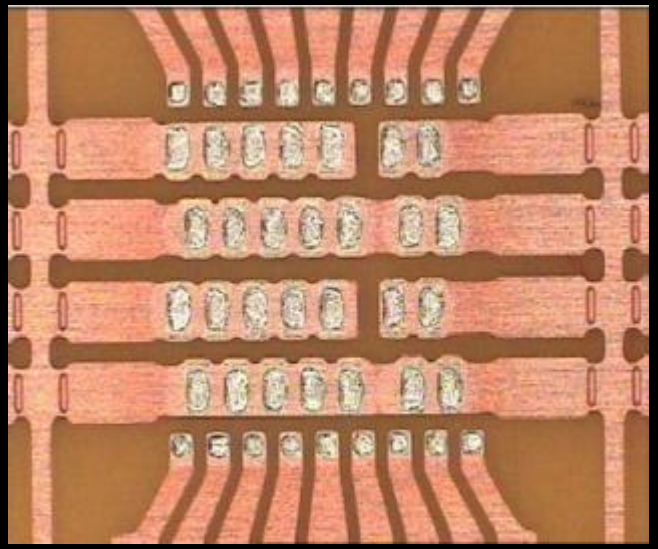
HOTROD™ – Flip chip Package for Power



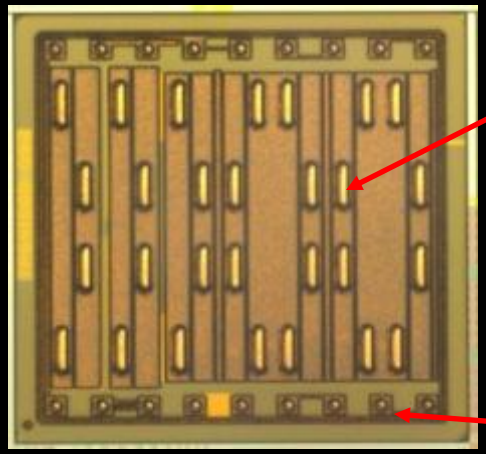
Package Bottom

Flip-Chip
Eliminates Wire
Resistance &
Wire Inductance





Leadframe



Cu bumps on die

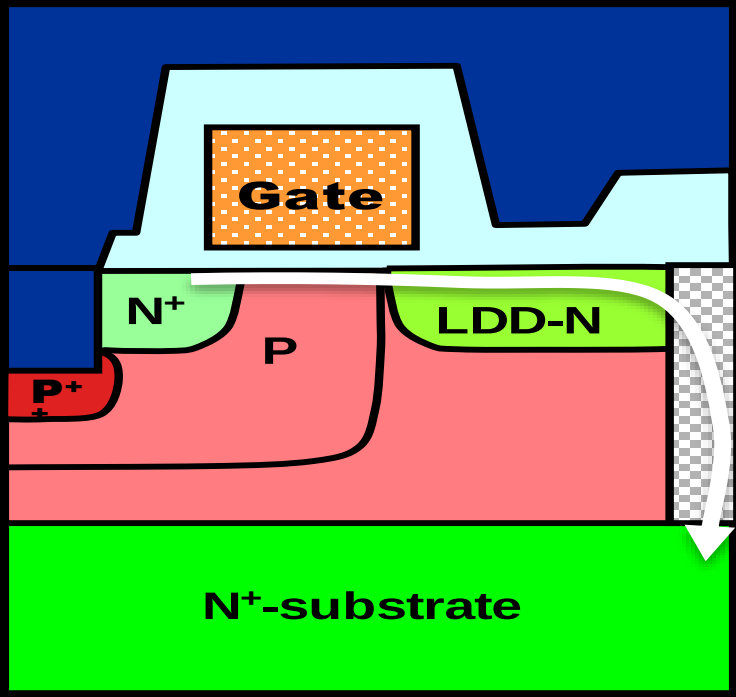
For Power Pins

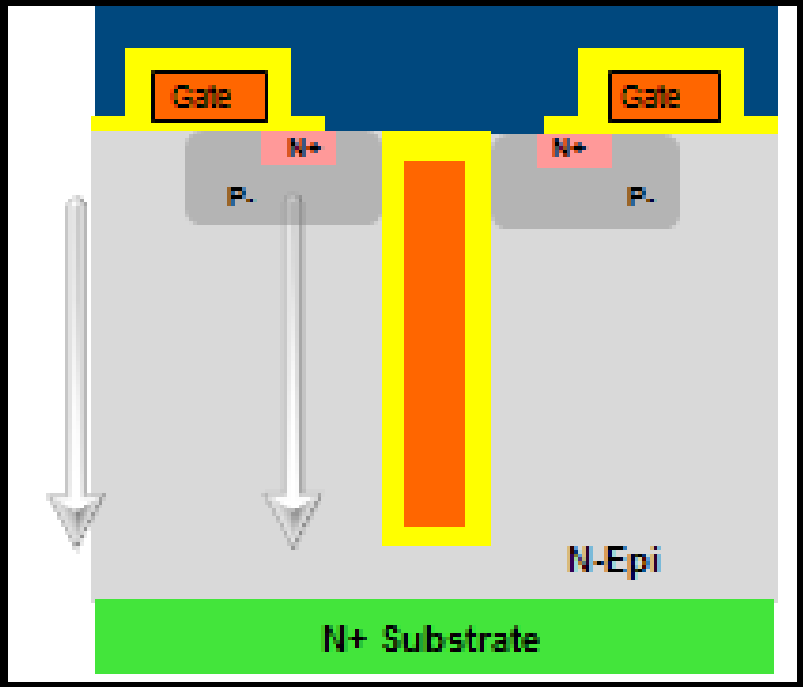
For Signal Pins

Outline

- Integrated LDMOS
- Isolation Requirements
- Interconnect & Packaging
- Discrete lateral DMOS & Packaging
  - Path towards higher current
  - Reduced design cycle time
  - Product flexibility
- Summary

Discrete FET Technology





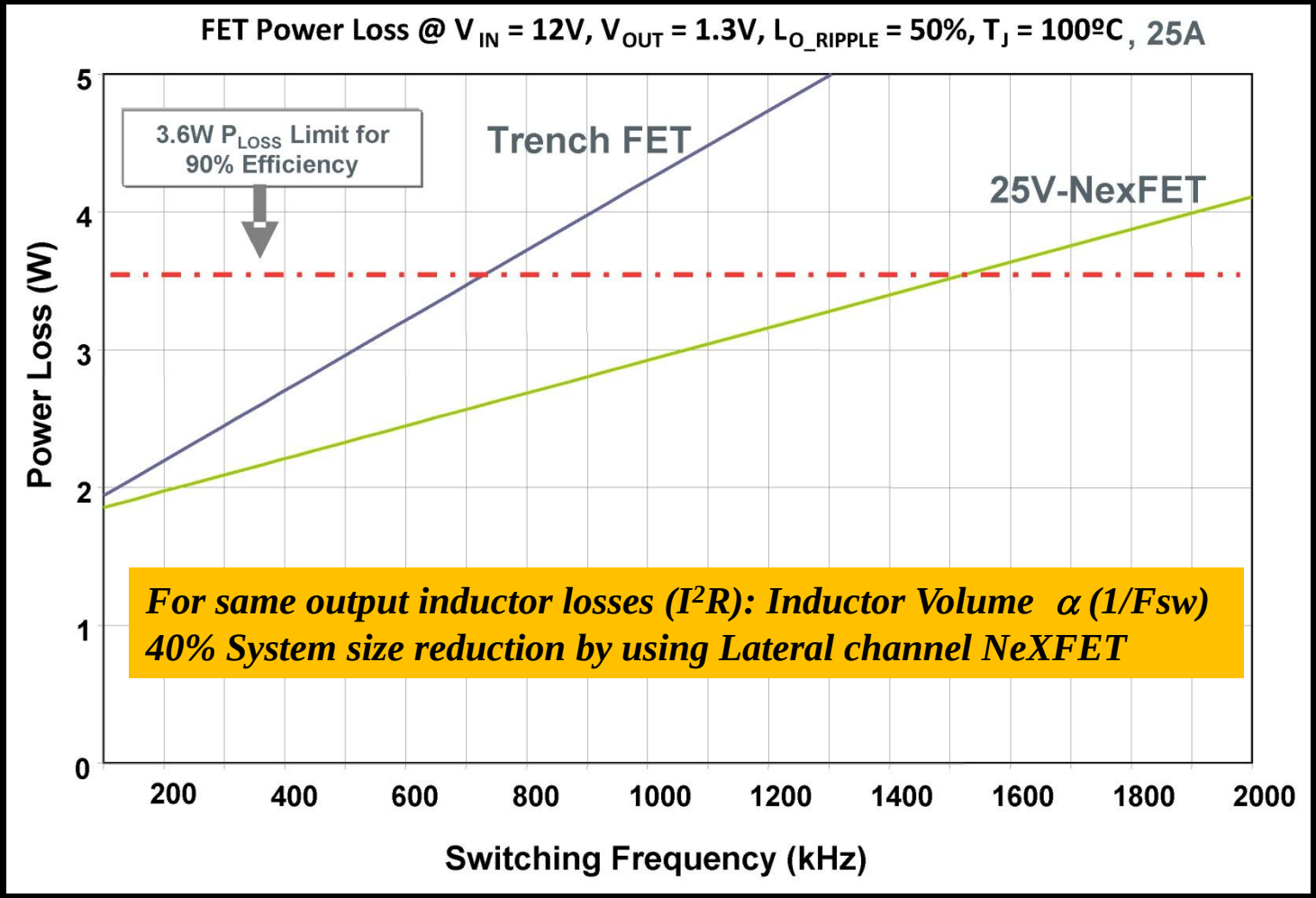
NexFET™ LV Technology

- LDMOS with Vertical Current Flow
- High density and low Rdson
- Low gate charge

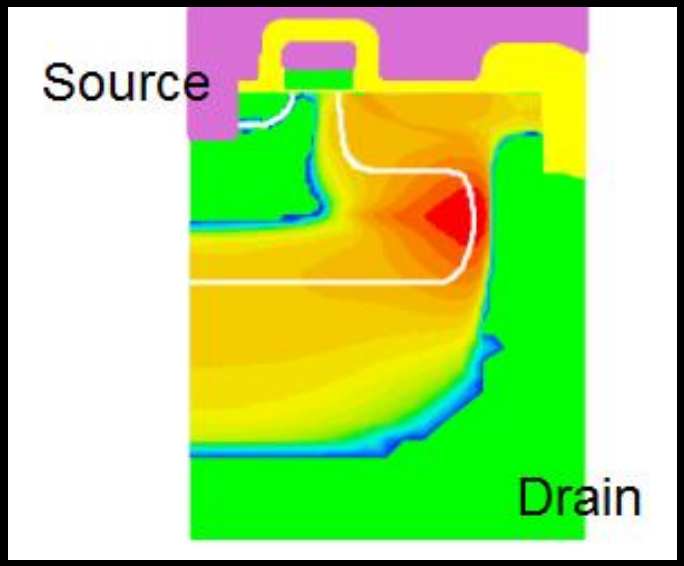
NexFET™ MV Technology

- Planar gate for low gate charge
- SJ Trench for lower Rdson
- Low gate charge & fast switching

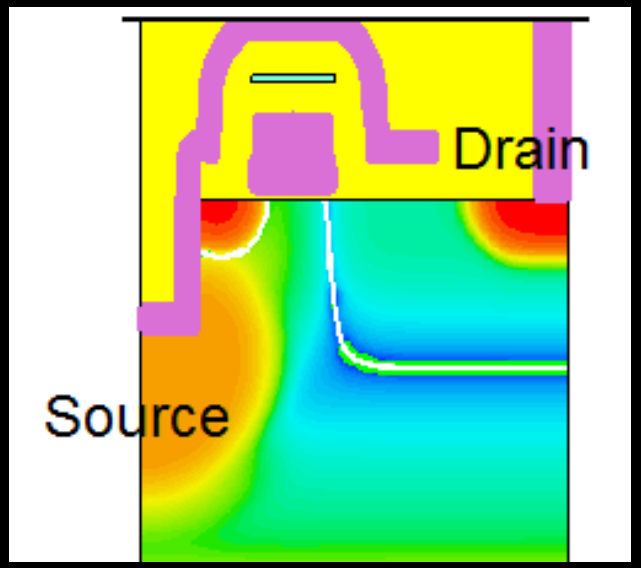
Power Loss vs. Frequency for Trench DMOS and NexFET



“Lateral” Discrete FET Flexibility



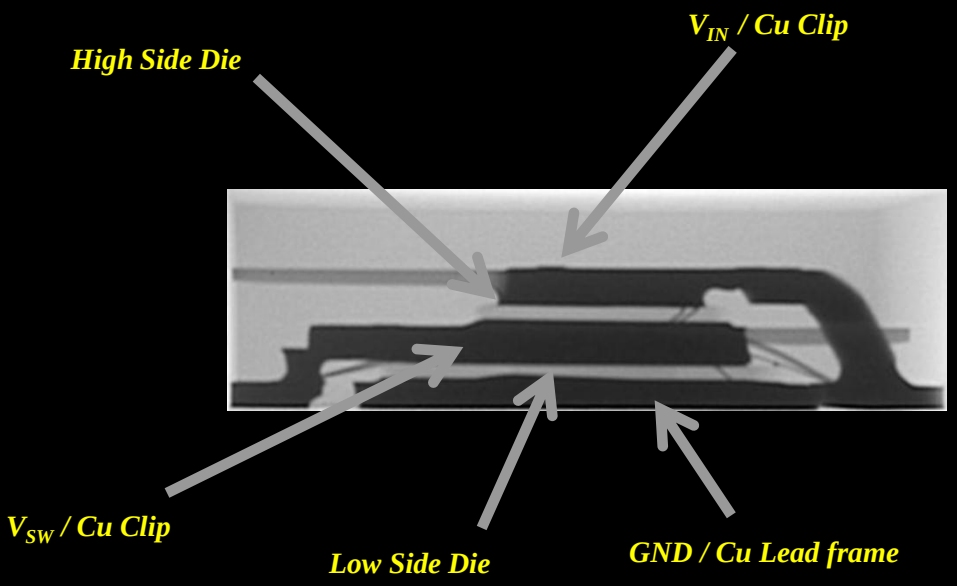
DRAIN DOWN

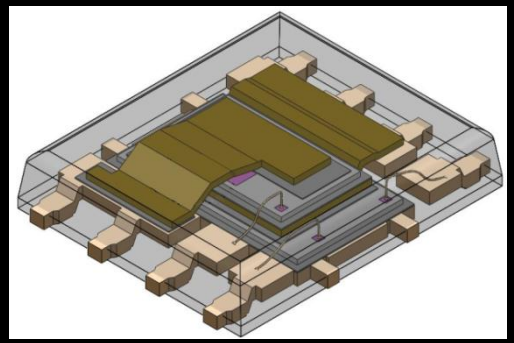


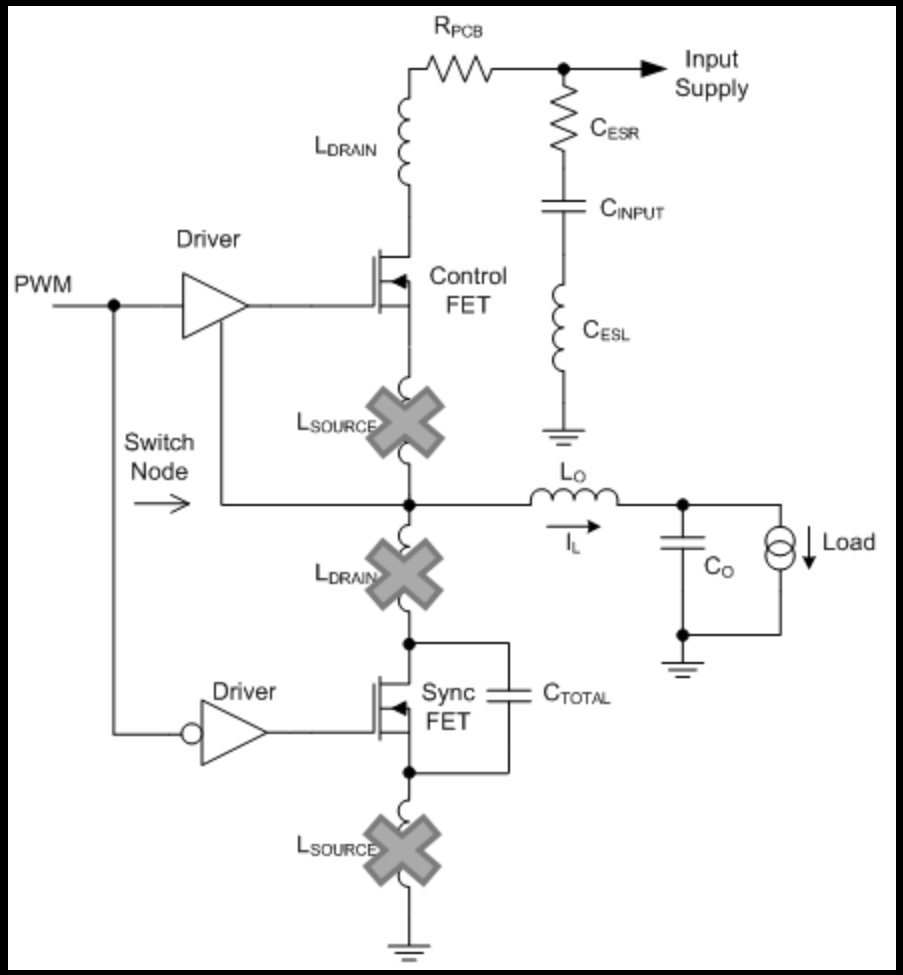
SOURCE DOWN

- Same architecture allows both “drain down” & “source down” structures
- Accomodates functional integration
  - Gate clamp, Gate segmentation, slew control

Stacked Die Packaging – Power Block

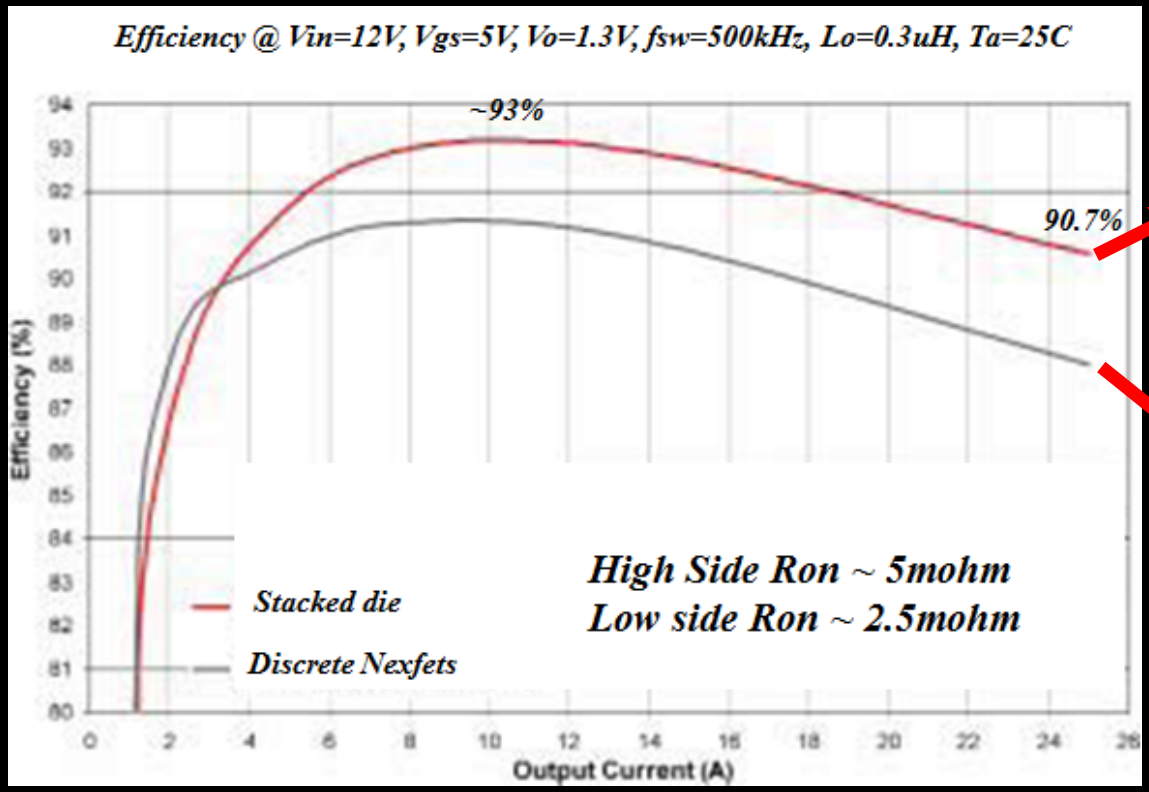






Stacked die reduces board space by more than 50%

Power Block – Efficiency Improvement



- About 20% reduction in losses with stacked die
- Similar die temperature/thermal performance

Summary

- Power conversion switching frequency increasing to enable footprint reduction
  - *Switching losses and diode losses more critical*
- Lateral power DMOS structure ideally suited
  - *Can be implemented as integrated or discrete*
- Lower gate and power loop as well as package inductances while maintaining high current interconnect
  - *Monolithic for low/mid current – flip chip*
  - *Stacked die for high current – Cu clip*

THANK YOU